PROGRESS IN PROGRAMMABLE LOGIC

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Summary Programmable logic devices (PLD) are situated on important place among microelectronic components thanks to the continuing technological development of semiconductor components, due to new architectures and new approaches to digital systems design. Software design of various complicated digital systems becomes advantageous article of many firms. The Department of Electronics and Electrotechnology pays permanent attention to mentioned components in application field. The collective of authors wants in this article point out on possibilities of design of digital system using the PLD. The paper plan contains the following basic parts: Technological aspects that influence development of configurable logic devices, Methodology of design and implementation and Flexibility of PLD interface.

1. INTRODUCTION

The Development of nanometer process technology at microelectronics leads to improvement of the PLD architectures. These advanced architectures enable to integrate complex electronic system on chip even though at small-scale production of electronic devices. New generations of the devices significantly extend flexibility of interfaces.

2. TECHNOLOGICAL DEVELOPMENT OF PLD

In the period of last five years the PLD production has broken the 100 nm technology border. Field Programmable Gate Array (FPGA) offer today 90 nm technology and as shown in Fig. 1 in one or two years we expect dealing with 50 nm technology. This trend is user positive in two aspects:

- Price reduction in relation with decrease of chip dimension (for example 80% by change from 130 nm to 90 nm technology).
- Improvement of both static and dynamic parameters and increase of capacity of built-in logic.

The architecture of new FPGAs consists of five basic programmable functional blocks:

- CLB (Configurable Logic Blocks). These blocks contain Look up Tables (LUT) realized as RAM (Random Access Memory). CLB allows to implement flip/flops, latches as logic and storage elements. CLBs are configured to perform a wide variety of logical and storage functions.
- IOB (Input/Output Blocks). These blocks control the data flow between the input/output(I/O) pins and the internal logic. Each IOB supports bi-directional data flow as well as 3-state operation. Wide range of different standards, including differential and high-performance I/O standards is available. DDR (Double Date Rate) registers are included too. The DCI (Digitaly Controlled Impedance) provides I/O terminations directly on chip.
- Block RAM. This memory is organized in the form of dual port blocks.
- Multiplier blocks. Multipliers calculate arithmetic multiplication accepting two binary words (up to 18 bit width).
- DCM (Digital Clock Manager). These important blocks operate in self-calibrating mode. Clock signal can be distributed with delay or phase shift into the whole chip. The base frequency can be multiplied or divided.

3. DESIGN AND IMPLEMENTATION OF PLD

The process of design and implementation of PLD is supported by effective, powerful design tools. The methodology of PLD is divided, as shown in Fig. 2

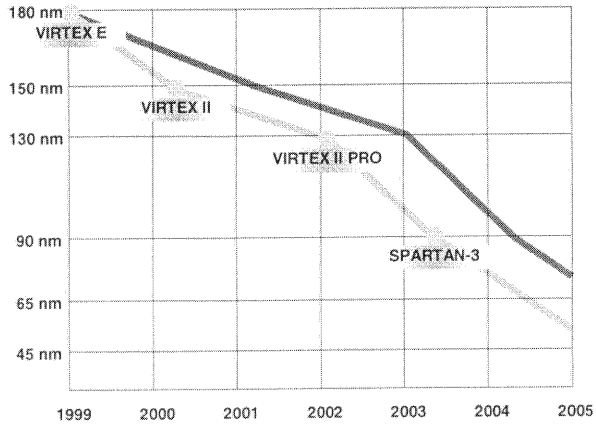

Fig. 1. World Class Process Microelectronic Technology Compared with Xilinx FPGAs.

into four steps: Design entry, Design Implementation, Verification of design and PLD programming.

3.1. Design entry

The first step can mean in a broader sense the following phases: feasibility study, conceptual design and design coding. The feasibility study specifies the function of device, algorithms of the function and discusses cost, rate and availability of the design. In the conceptual design the block diagram of device is created and technical demands

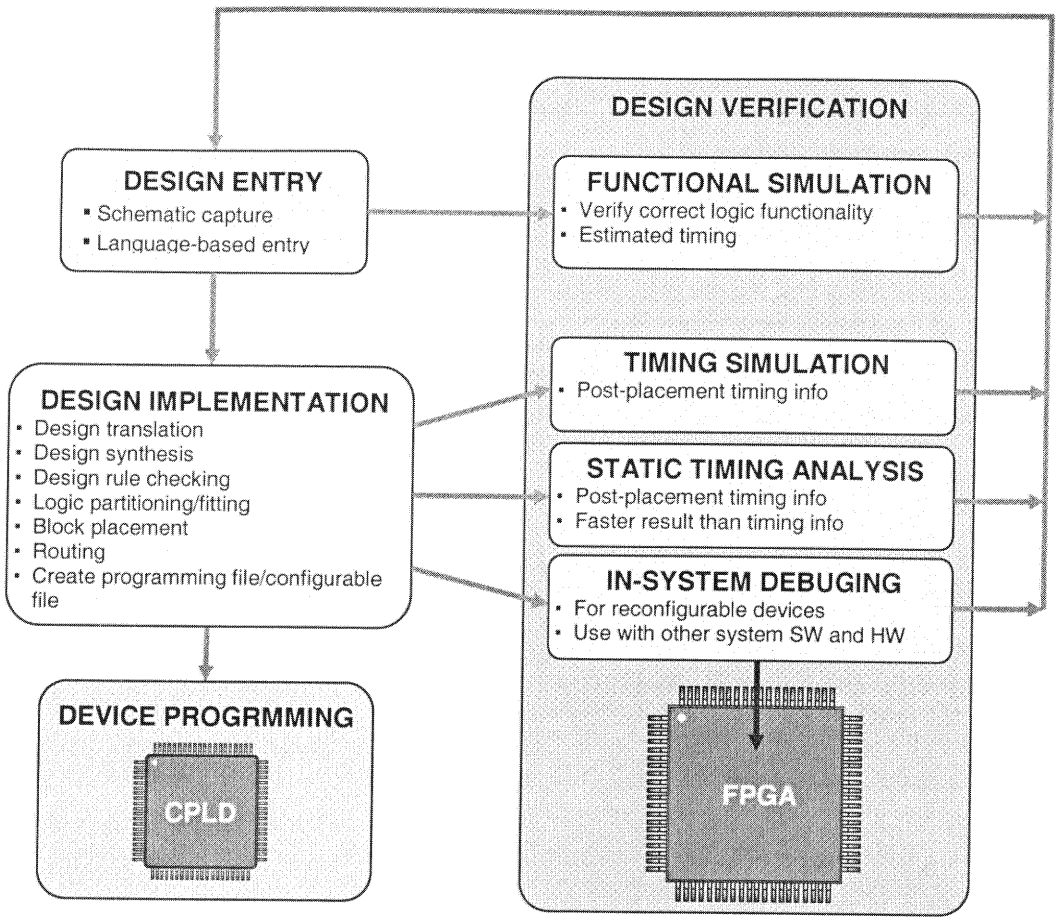

Fig. 2. Design flow of The Programmable Logic Devices.

on PLD are completed. For the possibility of further extensions, correction or reconfiguration of the device is necessary to create documentation of design phases. Design entry can be done using schematic entry package, or HDL (Hardware Description Language such as VHDL, Verilog), occasionally state diagram editor or using combination of the above mentioned eventualities. The PLD design is today supported by IPCs (Intellectual Property Cores). IP cores are predefined functions such as PCI bus interface, DMA controller ... The cores are verified and they can be directly implemented or adapted to given technology.

3.2. Design Implementation

Design tools convert the design entry into a netlist automatically. The netlist is in standard format that is readable for most implementation tools. After the translation the tools perform a design rules check and optimization on the incoming netlist. Then the software divides the design into logic blocks (LB) available on the device. Proper partitioning results in simpler routing and higher performance for the FPGAs and increased density and performance for the CPLDs (Complex Programmable Logic Devices). In next step the implementation software searches the best physical layout of the logic blocks. The goal is to reduce the amount of required routing resources. The implementation software monitors the routing length and routing track congestion while placing the LBs. The monitoring helps to calculate the absolute path delays in order to meet user specified timing constraints. In large applications the software may not be able to successfully place and route the design. Then the software offers more options. Designer uses the best one. To reach a successfully placed and routed design the software runs many iterations. Designer should try to use less than 85 % of the available device resources. It provides the software extra resources to help route the design. When the placement and routing process is complete, the software creates the binary programming file for configuration of the PLD.

3.3. Design Verification

The verification is very important part of the PLD design and occurs at all its phases. Designer applies more tools to verify the design function. Functional simulation is performed in conjunction with design entry, but before placing and routing, to verify correct logic functionality. Timing simulation is

performed after place and route. At that time the software back-annotates the logic and routing delays to the netlist for simulation. Static timing calculator provides faster results than timing simulation. Testing the design in the system is the final verification phase. ISP (In System Programmable) devices allow changes without costs even while the parts are mounted in the system. It is more easily to verify the design in system at full speed, with all of the hardware and software than to create the difficult and time consuming timing simulation. Some of device vendors supply in-system debugging tools capable to stop or single step the clock and to read back the state of internal flip-flops.

3.4. PLD programming

The created programming file configures the PLD. The programming method depends on the target technology. Most of the PLD producers use today ISP (In System Programmable) method through JTAG (Joint Test Action Group) interface.

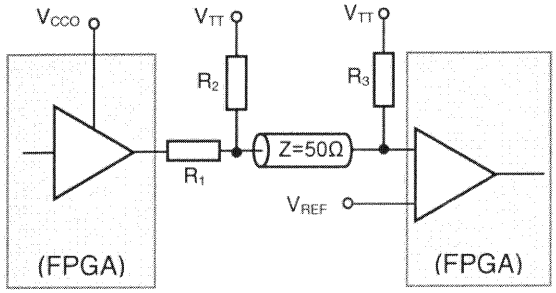

Fig. 3. Terminated Interface of the SSTL2 Class II. V_{TT}=1,25 V, R_1=25Ω, R_2=R_3=50Ω, V_{REF}=1,25 V, V_{CCO}=2,5 V.

4. FLEXIBILITY OF I/O INTERFACE OF FPGA

The demands on I/O interfaces of the FPGA grow according to their increasing complexity and performance. The variety of I/Os, the performance of I/Os and higher system clock frequency grow ever more. Low-voltage I/O standards are applied for the usage of low-voltage supply of integrated circuits.

4.1. External structure of I/O interface

External structure of I/O depends on the tolerance of allowed parameters of electrical quantities, on the form of conduction and on the form of termination of signal ways on printed circuits board PCB or between PCB boards. The most used I/O standards:

- LVTTL (Low Voltage Transistor Transistor Logic) is defined by the standard EIA/JEDEC for 3,3V, 2,5 V, 1,8 V supply.
- LVCMOS2 (Low Voltage Complementary Metal Oxide Semiconductor) is defined by the standard EIA/JEDEC for 3,3V, 2,5V, 1,8V, 1,5V voltage IC supply.

Tab. 1. Nominal Values of the Select I/O Supported Standard FPGAs

I/O Standard	Input Reference Voltage V_{REF} [V]	Output Source Voltage V_{CCO} [V]	External Termination Voltage V_{TT} [V]
LVTTL	unnecessary	3,3	unnecessary
LVCMOS2	unnecessary	2,5	unnecessary
PCI	unnecessary	3,3	unnecessary
GTL	0,8	unnecessary	1,2
GTL+	1,0	unnecessary	1,5
HSTL	0,75	1,5	0,75
HSTL	0,9	1,5	0,75
HSTL	0,9	1,5	0,75
SSTL	1,5	3,3	1,5
SSTL	1,25	2,5	1,25
CTT	1,5	3,3	1,5
AGP-2x	1,32	3,3	unnecessary
LVDS	unnecessary	1,5÷3,3	unnecessary

- PCI (Peripheral Component Interface) is defined by the standard PCI SIG for local PCI interface of personal microcomputers.
- GTL (Gunning Transceiver Logic) is defined by the standard EIA/JEDEC for fast busses.
- HSTL (High Speed Transceiver Logic) is defined by the standard EIA/JEDEC for transmitters and receivers of logical signal.
- SSTL (Stub Series Terminated Logic) is defined by the standard EIA/JEDEC for 3.3V or 2.5V for supply of the SRAM/DRAM busses.
- AGP (Advanced Graphics Port) is defined by the standard AGP forum for SRAM busses.
- LVDS (Low Voltage Differential Signaling) is defined by the standard EIA/JEDEC. The interface requires two pins of IC for inputs and outputs, but it has higher noise immunity opposite to the single ended I/O standards.
- BLVDS (Bus LVDS) is the bus connection of two or more circuits through differential signals.
- LVPECL (Low Voltage Positive Emitter Coupled Logic) is the ECL logic interface created by the differential signal.

High attention must be paid to the signal connections between the FPGAs on the PCB. Proper design of signal path eliminates unwanted electrical reflections and danger of electromagnetic emission. The correct termination of input and output pin of the FPGA is very important at high frequency of distributed logical signal. Fig. 3 shows an example of I/O termination of the FPGA using SSTL2 Class II interface. Table 1. shows which voltages (V_{REF}, V_{CCO}, V_{TT}) and in what level are necessary for certain I/O standard. Single-ended outputs do not require additive reference and terminations. Others, for example differential inputs need external reference voltage.

4.2. Internal structure of I/O interface

Configurable I/O blocks are allocated on the border of FPGA chip among banks of inputs and outputs, as shown in Fig. 4. Each bank has independent pin for

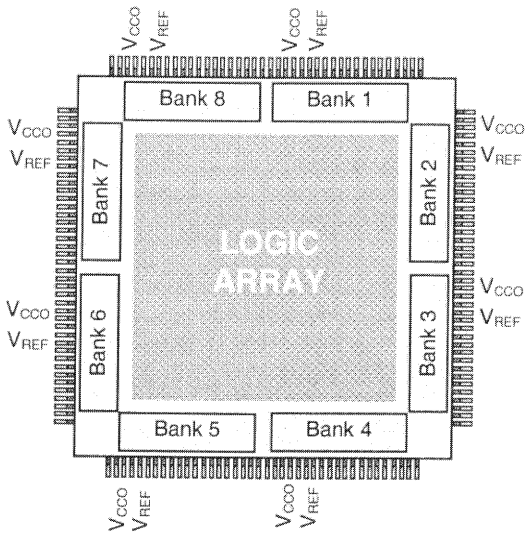

Fig.4. FPGA I/O Banks.

reference voltage of inputs V_{REF} and for voltage of outputs V_{CCO}. All inputs and outputs of one bank can be configured only for one I/O interface standard.
Each Input/Output Block (IOB) consists of three registers, one for the input, one for the output and 3-state signal register (Fig. 5). Such feature allows to configure the function of FPGA pins in addition to configuration of I/O standards. The FPGA can adjust other important attributes of input and output:

- drive strength output current,
- pull-up resistor,
- slew rate control,
- programmable delay of input, output signal path,
- open output circuitry,
- etc.

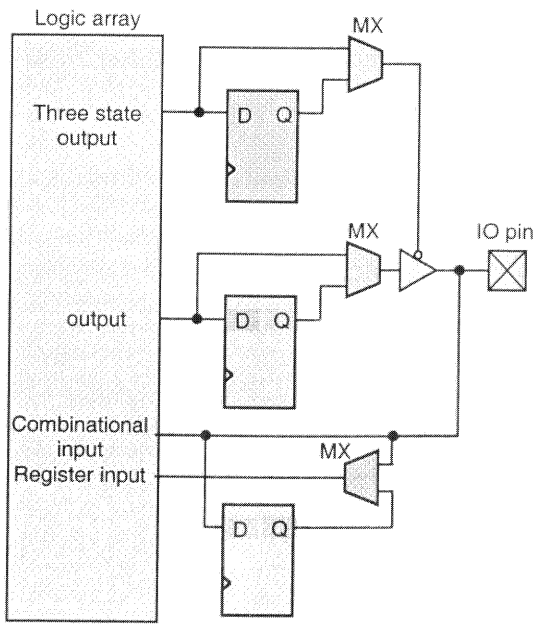

Fig. 5. The Option of the I/O function.

5. CONCLUSIONS

The development of microelectronics influences progress in PLD technology. The possibility to configure inputs and outputs to achieve I/O compatibility simplifies implementation of FPGA design. Flexible interfaces allow to realize wide spectrum of I/O applications, from universal interface standards (TTL, CMOS) to fast low-voltage interfaces often configured as busses. This feature simplifies connection of the FPGA with ICs like microprocessors, microcomputers, microcontrollers, semiconductor memories and other ASICs on PCB board or off PCB board.
Sophisticated development tools of PLD design and implementation into FPGA accelerate development of digital systems. Ever more FPGAs replace ASICs on their typical positions thanks to the advantageous price of the FPGAs.

REFERENCES

[1] HOLMBERG P.: Domain-Specific Platform FPGAs, FPGA and Programmable Logic Journal, January 6, 2004, Volume II, No. 1.

[2] ALFKE, P: Evolution and Revolution: Recent Progress in Field-Programmable, TechXclusives, September 2001.

[3] ČUNTALA, J., ŠINDLER, P., KONDELOVÁ, A.: The New Implementation Possibilities for Electronic Logical Devices, Advances in Electrical and Electronic Engineering, vol. 2/2003, No. 1 pp. 61-64.

[4] MALINIAK, D.: Tool Up for Alternatives to Standard ASICs, Electronic Design, September 15, 2003.

[5] JEDEC STANDARD , Solid State Technology Association 2000, 2500 Wilson Boulevard, Arlington, VA 22201-3834.

[6] ANSI/TIA/EIA-644. Electrical Characteristics of Low Voltage Differential Signaling, July 1995.